WHAT IS CLAIMED IS:

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1	1. A method for manufacture of a MOSFET device, the method comprising:
2	providing for a semiconductor substrate;

- providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;
- providing for a gate electrode in contact with at least a portion of the insulating layer;
 and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

- 2. The method of claim 1, wherein the MOSFET device is a planar P-type or N-type MOSFET, having any orientation.
- 3. The method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
- 4. The method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 5. The method of claim 1, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 6. The method of claim 1, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.
- 7. The method of claim 1, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 8. The method of claim 1, wherein dopants are introduced into the channel 2 region.

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- A method for manufacture of a MOSFET device, the method comprising: 9. 1 providing for a semiconductor substrate; 2 providing for an electrically insulating layer in contact with the semiconductor 3 substrate, the insulating layer having a dielectric constant greater than 7.6;
- providing for a gate electrode in contact with at least a portion of the insulating layer; 5 and 6
 - providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.
 - The method of claim 9, wherein the MOSFET device is a planar P-type or N-10. type MOSFET, having any orientation.
 - The method of claim 9, wherein the source and drain electrodes are formed 11. from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
 - The method of claim 9, wherein the source and drain electrodes are formed 12. from a member of the group consisting of the rare earth silicides.
 - The method of claim 9, wherein the insulating layer is formed from a member 13. of the group consisting of metal oxides.
 - The method of claim 9, wherein the Schottky contact or Schottky-like region 14. is formed at least in areas adjacent to the channel.
- The method of claim 9, wherein an entire interface between at least one of the 15. 1 source electrode and the drain electrode and the semiconductor substrate forms a Schottky 2 contact or Schottky-like region with the semiconductor substrate. 3
- The method of claim 9, wherein dopants are introduced into the channel 16. 1 region. 2

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substrate.

- A method for manufacture of a MOSFET device, the method comprising: 17. 1 providing for a semiconductor substrate; 2 providing for an electrically insulating layer in contact with the semiconductor 3 substrate, the insulating layer having a dielectric constant greater than 15; 4 providing for a gate electrode in contact with at least a portion of the insulating layer;
- and 6 providing a source electrode and a drain electrode in contact with the semiconductor 7 substrate and proximal to the gate electrode wherein at least one of the source electrode and 8 the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor 9
- The method of claim 17, wherein the MOSFET device is a planar P-type or N-18. 1 type MOSFET, having any orientation. 2
 - The method of claim 17, wherein the source and drain electrodes are formed 19. from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
 - The method of claim 17, wherein the source and drain electrodes are formed 20. from a member of the group consisting of the rare earth silicides.
 - The method of claim 17, wherein the insulating layer is formed from a 21. member of the group consisting of metal oxides.
- The method of claim 17, wherein the Schottky contact or Schottky-like region 22. 1 is formed at least in areas adjacent to the channel. 2
- The method of claim 17, wherein an entire interface between at least one of 23. 1 the source electrode and the drain electrode and the semiconductor substrate forms a 2 Schottky contact or Schottky-like region with the semiconductor substrate. 3
- The method of claim 17, wherein dopants are introduced into the channel 24. 1 2 region.

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silicide.

1	25. A method for manufacture of a MOSFET device, the method comprising:				
2	providing for a semiconductor substrate;				
3	providing for an electrically insulating layer in contact with the semiconductor				
4	substrate, the insulating layer having a dielectric constant greater than 4.0;				
5	providing for a gate electrode located in contact with at least a portion of the				
6	insulating layer;				
7	exposing the semiconductor substrate on one or more areas proximal to the gate				
8	electrode;				
9	providing for a thin film of metal on at least a portion of the exposed semiconductor				
10	substrate; and				
11	reacting the metal with the exposed semiconductor substrate such that a Schottky or				
12	Schottky-like source electrode and drain electrode are formed on the semiconductor				
13	substrate.				
1	26. The method of claim 25, wherein the MOSFET device is a planar P-type or N-				
2	type MOSFET, having any orientation.				
2	type wost E1, having any offentation.				
1	27. The method of claim 25, wherein the gate electrode is provided by:				
2	depositing a thin conducting film on the insulating layer;				
3	patterning and etching the conducting film to form a gate electrode; and				
4	forming one or more thin insulating layers on one or more sidewalls of the gate				
5	electrode.				
1	28. The method of claim 25, further comprising removing metal not reacted				
2	during the reacting process.				
2	during the reacting process.				
1	29. The method of claim 25, wherein the reacting comprises thermal annealing.				
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1	30. The method of claim 25, wherein the source and drain electrodes are formed				

31. The method of claim 25, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides. 2

from a member of the group consisting of: platinum silicide, palladium silicide and iridium

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- 1 32. The method of claim 25, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 33. The method of claim 25, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
- 1 34. The method of claim 25, wherein an entire interface between at least one of 2 the source electrode and the drain electrode and the semiconductor substrate forms a 3 Schottky contact or Schottky-like region with the semiconductor substrate.
- The method of claim 25, wherein dopants are introduced into the channel region.
- 1 36. A method for manufacture of a MOSFET device, the method comprising: 2 providing for a semiconductor substrate;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6;

providing for a gate electrode located in contact with at least a portion of the insulating layer;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

- The method of claim 36, wherein the MOSFET device is a planar P-type or Ntype MOSFET, having any orientation.
- 1 38. The method of claim 36, wherein the gate electrode is provided by:
- depositing a thin conducting film on the insulating layer;
- patterning and etching the conducting film to form a gate electrode; and
- forming one or more thin insulating layers on one or more sidewalls of the gate electrode.

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- 1 39. The method of claim 36, further comprising removing metal not reacted during the reacting process.
- 1 40. The method of claim 36, wherein the reacting comprises thermal annealing.
- 1 41. The method of claim 36, wherein the source and drain electrodes are formed
- 2 from a member of the group consisting of: platinum silicide, palladium silicide and iridium
- 3 silicide.
- 1 42. The method of claim 36, wherein the source and drain electrodes are formed 2 from a member of the group consisting of the rare earth silicides.
- 1 43. The method of claim 36, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
 - 44. The method of claim 36, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.
 - 45. The method of claim 36, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
 - 46. The method of claim 36, wherein dopants are introduced into the channel region.
- 1 47. A method for manufacture of a MOSFET device, the method comprising: 2 providing for a semiconductor substrate;
- providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;
- providing for a gate electrode located in contact with at least a portion of the insulating layer;
- exposing the semiconductor substrate on one or more areas proximal to the gate electrode;
- providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

- reacting the metal with the exposed semiconductor substrate such that a Schottky or
 Schottky-like source electrode and drain electrode are formed on the semiconductor
 substrate.
- 1 48. The method of claim 47, wherein the MOSFET device is a planar P-type or N-2 type MOSFET, having any orientation.
- 1 49. The method of claim 47, wherein the gate electrode is provided by:
- depositing a thin conducting film on the insulating layer;
- patterning and etching the conducting film to form a gate electrode; and
- forming one or more thin insulating layers on one or more sidewalls of the gate electrode.
- 1 50. The method of claim 47, further comprising removing metal not reacted during the reacting process.
- 1 51. The method of claim 47, wherein the reacting comprises thermal annealing.
- 1 52. The method of claim 47, wherein the source and drain electrodes are formed
- 2 from a member of the group consisting of: platinum silicide, palladium silicide and iridium
- 3 silicide.

- 53. The method of claim 47, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 1 54. The method of claim 47, wherein the insulating layer is formed from a
- 2 member of the group consisting of metal oxides.
- 1 55. The method of claim 47, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
- 1 56. The method of claim 47, wherein an entire interface between at least one of
- 2 the source electrode and the drain electrode and the semiconductor substrate forms a
- 3 Schottky contact or Schottky-like region with the semiconductor substrate.

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- The method of claim 47, wherein dopants are introduced into the channel region.
- 1 58. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
- 3 providing for a semiconductor substrate;
- providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;
- providing for a gate electrode in contact with at least a portion of the insulating layer;

 and
 - providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.
 - 59. The method of claim 58, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
 - 60. The method of claim 58, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 1 61. The method of claim 58, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 62. The method of claim 58, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
- 1 63. The method of claim 58, wherein an entire interface between at least one of 2 the source electrode and the drain electrode and the semiconductor substrate forms a 3 Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 64. The method of claim 58, wherein dopants are introduced into the channel 2 region.

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- 1 65. A method for manufacture of a device for regulating the flow of electrical
 2 current, the method comprising:
 3 providing for a semiconductor substrate;
 4 providing for an electrically insulating layer in contact with the semiconductor
 5 substrate, the insulating layer having a dielectric constant greater than 7.6;
 6 providing for a gate electrode in contact with at least a portion of the insulating layer;
 7 and
 - providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.
 - 66. The method of claim 65, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
 - 67. The method of claim 65, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
 - 68. The method of claim 65, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 69. The method of claim 65, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
- The method of claim 65, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- The method of claim 65, wherein dopants are introduced into the channel region.
- 1 72. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
- 3 providing for a semiconductor substrate;

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- providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;
- providing for a gate electrode in contact with at least a portion of the insulating layer;

 and
- providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- The method of claim 72, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
 - 74. The method of claim 72, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- The method of claim 72, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
 - 76. The method of claim 72, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.
 - 77. The method of claim 72, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- The method of claim 72, wherein dopants are introduced into the channel region.
- 1 79. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
- 3 providing for a semiconductor substrate;
- providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;

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6	providing for a gate electrode located in contact with at least a portion of the
7	insulating layer;
8	exposing the semiconductor substrate on one or more areas proximal to the gate
9	electrode;
10	providing for a thin film of metal on at least a portion of the exposed semiconductor
11	substrate; and
12	reacting the metal with the exposed semiconductor substrate such that a Schottky or
13	Schottky-like source electrode and drain electrode are formed on the semiconductor
14	substrate.

- 1 80. The method of claim 79, wherein the gate electrode is provided by:
 2 depositing a thin conducting film on the insulating layer;
 3 patterning and etching the conducting film to form a gate electrode; and
 4 forming one or more thin insulating layers on one or more sidewalls of the
 5 gate electrode.
 - 81. The method of claim 79, further comprising removing metal not reacted during the reacting process.
 - 82. The method of claim 79, wherein the reacting comprises thermal annealing.
 - 83. The method of claim 79, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
- 1 84. The method of claim 79, wherein the source and drain electrodes are formed 2 from a member of the group consisting of the rare earth silicides.
 - 85. The method of claim 79, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 86. The method of claim 79, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.

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1	87. The method of claim 79, wherein an entire interface between at least one of				
2	the source electrode and the drain electrode and the semiconductor substrate forms a				
3	Schottky contact or Schottky-like region with the semiconductor substrate.				
1	88. The method of claim 79, wherein dopants are introduced into the channel				
2	region.				
1	89. A method for manufacture of a device for regulating the flow of electrical				
2	current, the method comprising:				
3	providing for a semiconductor substrate;				
4	providing for an electrically insulating layer in contact with the semiconductor				
5	substrate, the insulating layer having a dielectric constant greater than 7.6;				
6	providing for a gate electrode located in contact with at least a portion of the				
7	insulating layer;				
8	exposing the semiconductor substrate on one or more areas proximal to the gate				
9	electrode;				
10	providing for a thin film of metal on at least a portion of the exposed semiconductor				
11	substrate; and				
12	reacting the metal with the exposed semiconductor substrate such that a Schottky or				
13	Schottky-like source electrode and drain electrode are formed on the semiconductor				
14	substrate.				
1	90. The method of claim 89, wherein the gate electrode is provided by:				
2	depositing a thin conducting film on the insulating layer;				
3	patterning and etching the conducting film to form a gate electrode; and				
4	forming one or more thin insulating layers on one or more sidewalls of the gate				
5	electrode.				
1	91. The method of claim 89, further comprising removing metal not reacted				
2	during the reacting process.				

The method of claim 89, wherein the reacting comprises thermal annealing.

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1	93.	The method of claim 89, wherein the source and drain electrodes are formed
2	from a member	er of the group consisting of: platinum silicide, palladium silicide and iridium
3	silicide.	

- 1 94. The method of claim 89, wherein the source and drain electrodes are formed 2 from a member of the group consisting of the rare earth silicides.
- 1 95. The method of claim 89, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 96. The method of claim 89, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
 - 97. The method of claim 89, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 98. The method of claim 89, wherein dopants are introduced into the channel 2 region.
 - 99. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
- providing for a semiconductor substrate;
- providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;
- providing for a gate electrode located in contact with at least a portion of the insulating layer;
- exposing the semiconductor substrate on one or more areas proximal to the gate electrode;
- providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

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12	reacting the metal with the exposed semiconductor substrate such that a Schottky or
13	Schottky-like source electrode and drain electrode are formed on the semiconductor
14	substrate.

- 1 100. The method of claim 99, wherein the gate electrode is provided by:
- depositing a thin conducting film on the insulating layer;
- patterning and etching the conducting film to form a gate electrode; and
- forming one or more thin insulating layers on one or more sidewalls of the gate electrode.
- 1 101. The method of claim 99, further comprising removing metal not reacted during the reacting process.
- 1 102. The method of claim 99, wherein the reacting comprises thermal annealing.
- 1 103. The method of claim 99, wherein the source and drain electrodes are formed 2 from a member of the group consisting of: platinum silicide, palladium silicide and iridium 3 silicide.
 - 104. The method of claim 99, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
 - 105. The method of claim 99, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 106. The method of claim 99, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
- 1 107. The method of claim 99, wherein an entire interface between at least one of 2 the source electrode and the drain electrode and the semiconductor substrate forms a 3 Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 108. The method of claim 99, wherein dopants are introduced into the channel 2 region.